digital INTEROFFICE MEMORANDUM

DATE: October 27, 1969

SUBJECT: Design Review Minutes of October 20, 1969

TO: Roger Cady
Jim O'Loughlin
PDP-11 Design Review Committee

FROM: Grant Saviers

1. Edge delays and pulse circuits as used in the PDP-11 were discussed. It was pointed out that current limiting is required on edge delays.

2. A careful worst-case analysis of all pulse circuits is required. Special attention should be paid to temperature stability and differences between "compatible" TTL sources. Dick Best pointed out that Signetics and TI gates have quite different (although within specification) characteristics.

3. In general the committee approves of the documentation to be provided as "logic prints". The block circuit concept seems reasonable if a wire list is provided in the print set.

4. Jim O'Loughlin agreed that a presentation of the processor organization will be made before the committee goes "signal chasing" on the prints.

/sm

Present: D. Best
G. Fligg
H. Spencer
J. O'Loughlin
G. Saviers

Design Review Committee:

G. Butler
A. Kotok
R. Pyle
D. Dubay
H. Godfrey
I. Morris